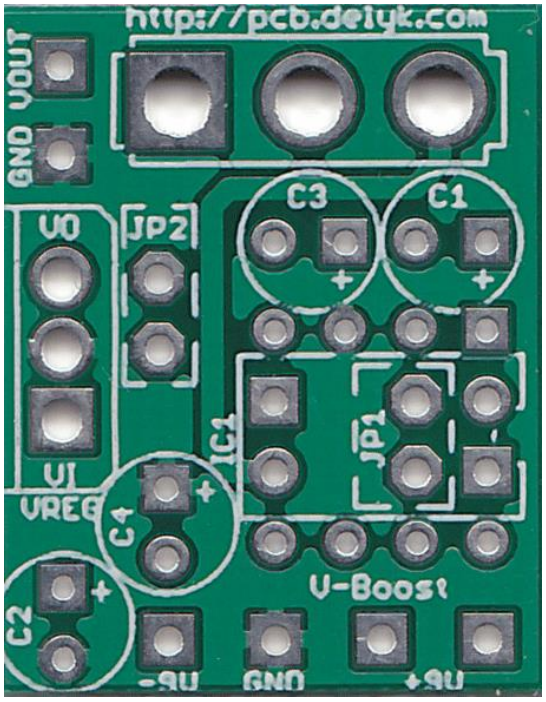


V-Boost

Build Document

Bill of Materials

Capacitors

I obtained all of my capacitors from Tayda. That's what the layout was setup for.

P/N	Value	Type	Notes
C1	10uF	Aluminum Electrolytic	50V. If using -9V, remove.
C2	10uF	Aluminum Electrolytic	50V. If using -9V, remove.
C3	10uF	Aluminum Electrolytic	50V. If using -9V, remove.
C4	47uF	Aluminum Electrolytic	At least 16V. If not using -9V, remove.

Diodes

I obtained all of my diodes from Tayda. That's what the layout was setup for.

P/N	Value	Notes
D1	1N5817	If using -9V, remove.
D2	1N5817	If using -9V, remove.

Integrated Circuits

I obtained all of my ICs from Tayda. That's what the layout was setup for.

P/N	Value	Notes
IC1	MAX1044/7660S/LT1054	If you use the LT1054, keep JP1 open. If you use MAX1044 or 7660S, jump JP1.
VREG	7812/7815 Voltage Regulator	Optional. Use this only if you want to cap your voltage at something greater than 9V and lower than 18V. **If you do not use a vreg, jump JP2.**

Other Parts

I obtained all of these from Tayda. That's what the layout was setup for.

Qty	Value	Notes
1	SPDT On-On Switch	

Build Notes

- ~~I got shocked badly once near the charge pump.~~ ~~**Be careful.**~~ Turns out, it was the same bad IC from my Effects Tester Mk II.
- Be careful to measure heights! Depending on enclosure size and location, you may want to put the SPDT on the same side as the IC/caps.
- Includes an extra +9V pad so you can daisy chain off it if you wish.

Suggested Solder Order

1. If JP1 is necessary (based on your IC), solder this before anything else.
2. Solder D1 and D2.
3. If JP2 is necessary (because you're not using a VREG), solder this.
4. Solder IC1.
5. Solder the rest.

Usage

-9V Only

C4 only. D1 and D2. (JP1?) IC1. Ignore VREG. Ignore JP2. Ignore VOUT. Ignore VSELECT. Wire your input +9V and GND. Use -9V for the output.

12V/15V Only

C1, C2, and C3. D1 and D2. (JP1?) IC1. Add a VREG (7812/7815). Ignore JP2. Jump square pad to middle pad of VSELECT. Wire your input +9V and GND. Use VOUT and GND for the output.

18V Only

C1, C2, and C3. D1 and D2. (JP1?) IC1. Ignore VREG. Jump JP2. Jump square pad to middle pad of VSELECT. Wire your input +9V and GND. Use VOUT and GND for the output.

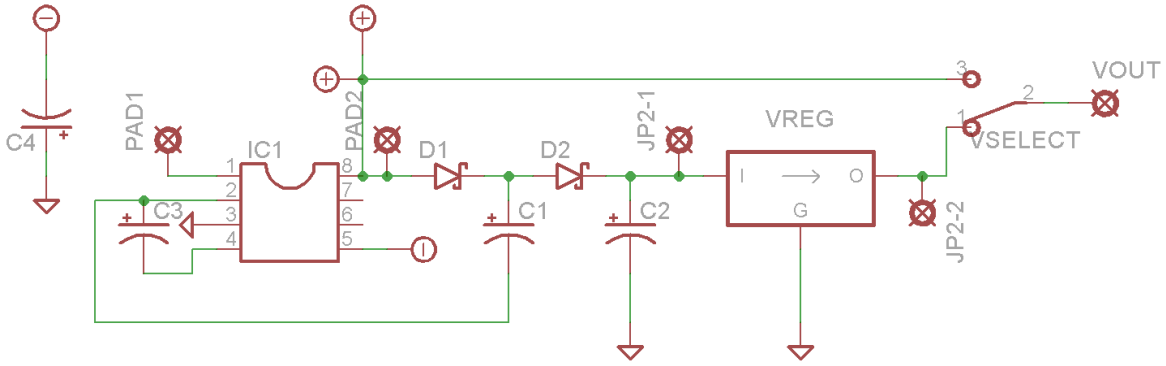
9V and 12V/15V (Switchable)

C1, C2, and C3. D1 and D2. (JP1?) IC1. Add a VREG (7812/7815). Ignore JP2. Add SPDT for VSELECT. Wire your input +9V and GND. Use VOUT and GND for the output.

9V and 18V (Switchable)

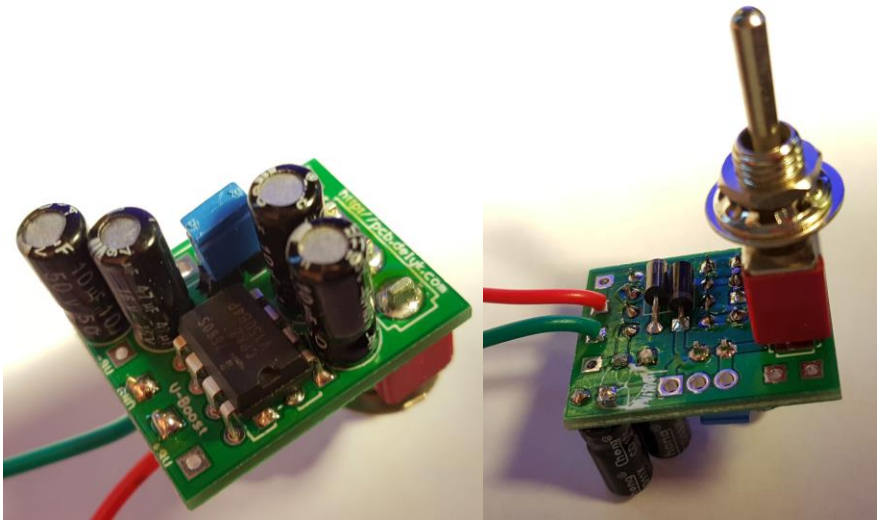
C1, C2, and C3. D1 and D2. (JP1?) IC1. Ignore VREG. Jump JP2. Add SPDT for VSELECT. Wire your input +9V and GND. Use VOUT and GND for the output.

Schematic


C4
PAD1
IC1
PAD2
D1
D2
JP2-1
VREG
VOUT
VSELECT
C3
C1
C2
JP2-2
I
O
G
1
2
3
4
5
6
7
8

Images

Standard Configuration



Minimal Configuration

Notice the bending of the caps. This will reduce your footprint in a tight enclosure.